

iPS-SWREG-WS25

High Speed ATE Load Board Regulator

Features

- Programmable 0-3.0V, 25A regulator
- Less than 30mV voltage droop for 25A/nsec di/dt load change
- Low Dropout Voltage (< 500mV for 25Amp output) reduces power dissipation
- Iout measured directly by ATE supply source
- Small board size: 2.0"W 2.8"L 0.7"H
- Pluggable for easy installation and removal
- Over-temperature auto shut-down and status signal
- Voltage shut-down control independent of programmed Vout value

Applications

- ATE Equipment
- ATE Load Boards

Description

The iPS-SWREG-WS25 is a small, high speed 0-3.0V, 25A regulator board suitable for plugging into ATE load boards close to the Device Under Test (DUT). This high-speed regulator responds to di/dt demands much faster than the typical ATE supply is capable of doing.

The fast response of the regulator allows a significant reduction in the total value of the decoupling capacitance required to keep the DUT voltage constant despite large and fast di/dt changes (25A /nsec). This capacitance value can often be reduced by a factor of 100 or more for a given DUT di/dt step load change and voltage droop requirement.

Typical Application

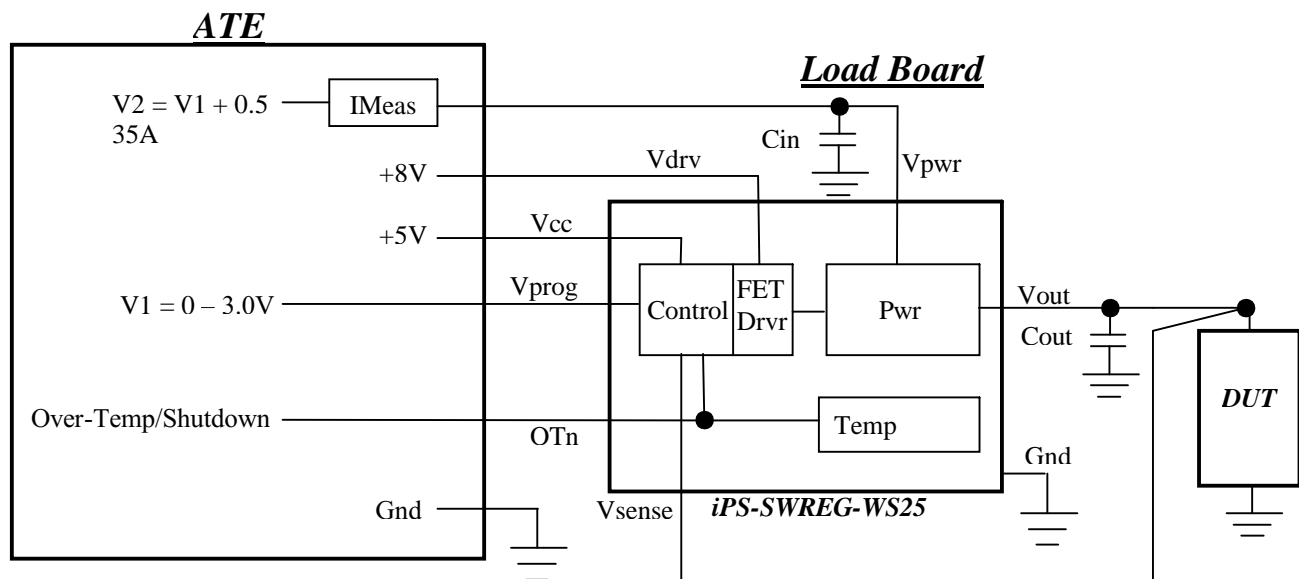


Fig. 1



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DC Specifications

Vdrv	Min-Max voltage range (nominal 8.0 Volts)	0 – 8.5 Volts @ up to 2A
Vcc	Min-Max voltage range (nominal 5.0 Volts)	4.5 – 5.5 Volts @ up to 1A
Vprog	Min-Max voltage range	0 – 3.0 Volts
Vpwr	Min-Max voltage range (nominal Vprog + 0.5V)	0 – 3.5 Volts up to 25A
Vsense	Min-Max external Vout sense range	0 – 3.0 Volts
Vout	Maximum voltage range	0 – 3.0 Volts
OTn	Maximum input or output over-temp signal	0 – 5.0 Volts (open collector with 10K pull up to 5V)
Ppwr	Maximum input power Iout X Vdrv	87.5 Watts
Pout	Maximum power output Iout X Vout	75.0 Watts
Regulator Efficiency	Maximum regulator efficiency	75%
Ppw – Pout	Maximum heat sink power dissipation with fan running	15 watts
Tboard	Maximum board temperature for auto shutdown	85 degrees C (3 degrees hysteresis)

Vcc = 5.0V, Vdrv = 8.0V, T=25 degrees C

Parameter	Type	Description	Min	Max	Units
Idrv	I	Pre-driver current with Vdrv @ 8.0 volts	0.02	2	A
Icc	I	Fan + over-temp circuit current		1	A
Vprog	I	Programming pin used to set the output voltage	0	3.0	V
Iprog	I	Programming signal input current		10	mA/V
OTn output high	I/O	High level indicates board temperature OK	Vcc – 0.4	VCC	V
OTn output low	I/O	Low level indicates board temperature exceeded	0	0.4	V
OTn input	I/O	Drive input low to disable Vout to zero volts (open collector with 10K pull up resistor)	0	0.8	V
Vsense	I	External sense input pin voltage range	Vout	Vout	V
Isense	I	External sense input pin input current	0	10	mA/V
Vout	O	Output voltage tracks Vprog	Vprog-0.02	Vprog+0.02	V
Iout	O	Output current	0	25	A
Vpwr	I	Power regulator voltage	0	Vprog+0.5	V
Ipwr	I	Power regulator current	0	25+Vprog/100	A



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AC Parameters

Vcc = 5.0V, Vdrv = 8.0V, T=25 degrees C (see note 2)

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Units</i>
TVoutH	Ramp Vout to new higher Vprog (<i>Note 1</i>)	$(I_{lim} - I_{dut} - V_{out}/100)/C_{out}$	V/sec
TVoutL	Ramp Vout to new lower Vprog (<i>Note 1</i>)	$-(I_{dut} - V_{out}/100)/C_{out}$	V/sec
Tpwrap	Time for the regulator to stabilize after VCC and Vdrv are applied	10	msec
Voutdi/dt	Regulation for 25A/nsec current demand	+/- 30 (<i>Note 3</i>)	mV
Tresp	Time for full recovery after 25A/nsec transient load	1	usec

Note 1: I_{lim} is the current limit set on the Vpwr power supply. Normally set this to $I_{out\ max} + 10A$. C_{out} is the total DUT decoupling capacitance. The ramp time is valid for small changes (<200mV) in Vprog. Larger changes may be affected by Cin input decoupling capacitance.

Note 2: Regulator power-on sequence is: Vcc, Vdrv, Vpwr and then Vprog. Vcc and Vdrv should remain on at all times after the initial power-on sequence. Vcc powers the cooling fan as well as the over-temperature and shut-down circuitry while Vdrv powers the regulator and FET pre-driver circuits. Vpwr is programmed to 0.5V above Vprog and must track Vprog at all times.

Note 3: This droop/overshoot specification assumes adequate Cin and Cout decoupling and good layout practices have been followed. See “Recommended Decoupling” section.

Regulator Board Operation

See the figure 2 below. A control block takes an input voltage, Vprog, and compares it to Vout, which is fed back through the Vsense pin. The difference in voltage between Vout and Vprog is amplified and applied to a FET driver, which in turn drives the Pwr block in such a way that Vout is forced to equal Vprog. Current through the Pwr block from Vpwr goes directly to a load connected to Vout. This allows output current to be directly measured from the Vpwr source. There is a small constant load of 100 ohms on Vout, which must be taken into account.

A temperature sensor measures the temperature of the board near the Pwr stage and if this temperature exceeds 85 degrees C, a signal is sent to the Control block which forces Vout to zero volts. At the same time, this signal, OTn, is brought to an external pin that can be sampled to determine if the board is in a temperature shutdown state. A high state indicates that the temperature on the board is OK. This sensor will recover when the temperature drops back below 82 degrees C.

Additionally, this same over-temperature pin, OTn, can be used to force a shutdown state by forcing it low. This pin is internally connected to an open collector driver with a 10k pull-up resistor so any external tri-state or open collector driver can drive this pin low to put it into the shutdown state.

The regulator power-on sequence is to turn on Vcc, Vdrv, Vprog and Vpwr in that order, spaced about 1msec apart. The regulator will stabilize in less than 10msec. Vcc and Vdrv should remain on for the duration of a test session with Vprog and Vpwr being programmed as required to drive the DUT. Vcc is used to drive the cooling fan so it is critical for it to remain on at all times. Vpwr should be set to Vprog + 0.5V for normal operation.

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Regulator Block Diagram

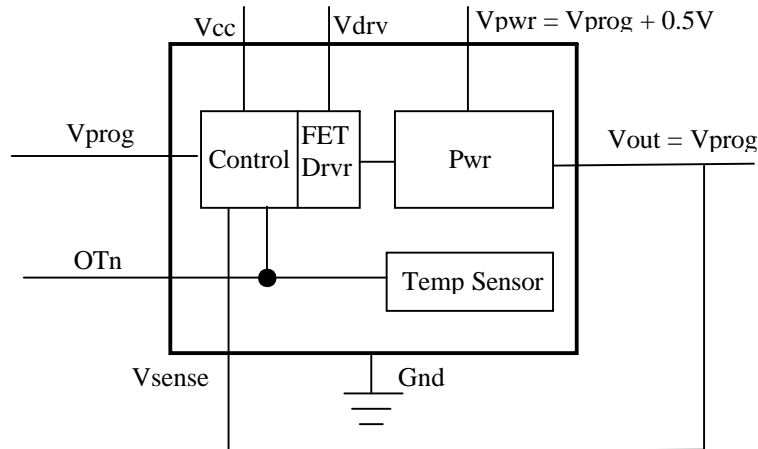


Fig. 2

The Advantage of a Fast Local Regulator

Modern telecom, video and processor chips switch from the inactive mode to the active mode in a very short time period. This generates very fast current changes of up to 25A/nsec or more. ATE power supplies and local decoupling capacitors must supply the current that these fast load changes demand while maintaining voltage levels within DUT operating specifications so as to not lose data at these transitions.

Typical high-end ATE power supplies are slow, in the range of 100 to 500 microseconds response time and some even slower. Even if they are faster, they are still too far from the DUT to take advantage of it because of series inductance between the supply and the DUT or load board connection. The usual solution is to place a “ton of decoupling capacitors” close to the DUT on the load board to supply the demanded load current until the power supply can react.

A typical ATE power supply vendor with 200usec response time recommends decoupling capacitance values of about 5000uF per 5A of transient current demand to guarantee no more than 200mV of droop until the power supply can take over. For a fast load transient of 25A, about 25,000uF of capacitance will be required to hold up the DUT voltage 200usec while keeping the droop less than 200mV.

For modern low voltage devices, a droop specification of less than 25-30mV is desirable. If the decoupling capacitance is doubled to 50,000uF, the droop voltage will be ½ of 200mV or 100mV. Continue this process and you end up with a required capacitance of 200,000uF for a 25mV droop. Unfortunately it’s even worse than that. Since real capacitors have parasitic series resistance and series inductance, you must account for any undesirable droop or overshoot problems due to these elements. The general solution requires many, many high quality capacitors in parallel totaling 200,000uF or more. Another side effect of large total values of capacitance is that the ATE power supply may start to ring or even oscillate not to mention that the time to ramp the supply voltage up and down has gotten much longer.

As anyone knows who has put 200,000uF of high quality, high frequency capacitors on a load board, it is difficult, expensive and hard to maintain. Using a fast, local regulator will significantly reduce the requirement for these large total capacitance values.

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Recommended Decoupling for iPS-SWREG-WS25

The typical iPS-SWREG-WS25 application diagram shown on page 1 shows two main decoupling capacitors, Cin and Cout. These decoupling capacitors are actually many capacitors connected in parallel. Cin must guarantee that the power supply voltage from the ATE does not droop more than about 200mV at the input to the regulator. Cin typically requires 25,000uF for 25A of fast load change and must support a moderate bandwidth. Cout requires 2200uF for all cases up to Iout of 25A and must have a wide bandwidth to deal with a fast load change (25A/nsec).

To achieve a 30mV voltage droop/overshoot specification, the impedance of the Cout decoupling array must be kept below 1.2 milliohm ($Z = V/I$) across a wide frequency band. The low end of the bandwidth is approximately $f_l = 300/T_{resp}$ where f_l is in MHz and T_{resp} is in nsec. So $f_l = 300/1000 = 0.3\text{MHz}$ or 300KHz. Similarly, the high end of the bandwidth is $f_h = 300/1\text{nsec} = 300\text{MHz}$ to support 25A/nsec load changes. Achieving 300MHz is very hard to do on a load board. Via inductance in series with the decoupling capacitors is often the high frequency limiting factor and care must be taken to insure that this inductance is minimized during layout and taken into account in the impedance calculations.

This wide bandwidth Cout decoupling is accomplished by placing a large number of small valued capacitors in parallel to total 2200uF. Shown below in figures 3, 4 and 5 are graphs that show impedance vs. frequency curves for various combinations of capacitors for the Cout array. These graphs account for board vias that are 0.7nH on both sides of the decoupling capacitors. Using double vias will reduce the number of capacitors required for a given bandwidth. All capacitors shown must satisfy $esr/N \leq 500\text{micro ohms}$, where esr is the equivalent series resistance of the capacitor type and value and N is the number of that type and value. All equivalent series inductance (esl) values should be $\leq 1\text{nH}$ for each capacitor type and value as well.

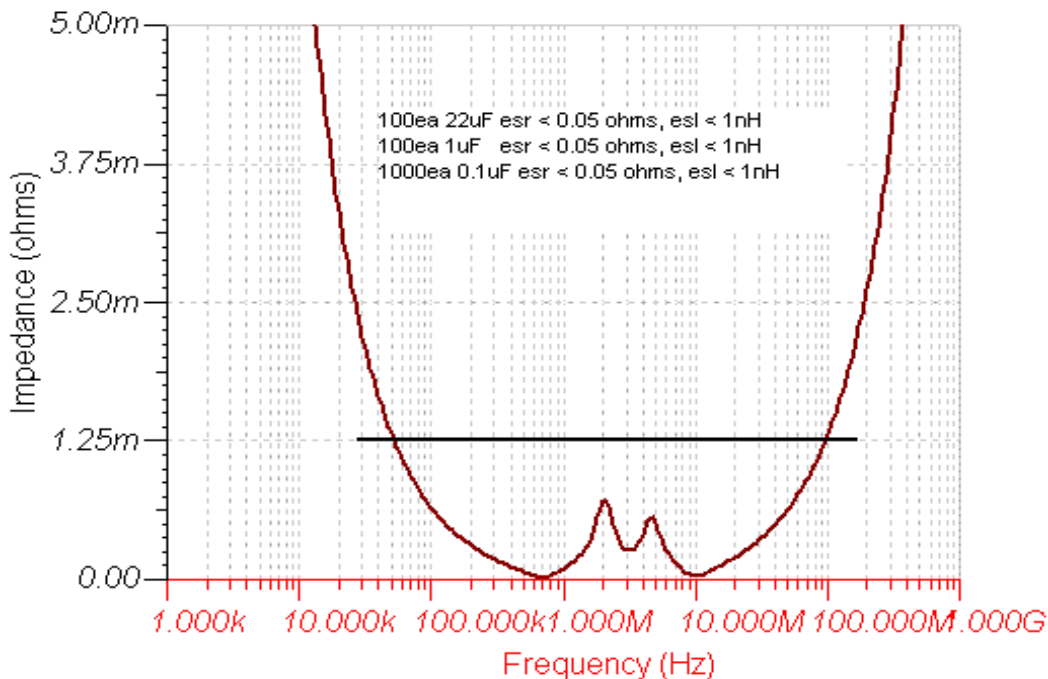


Fig. 3



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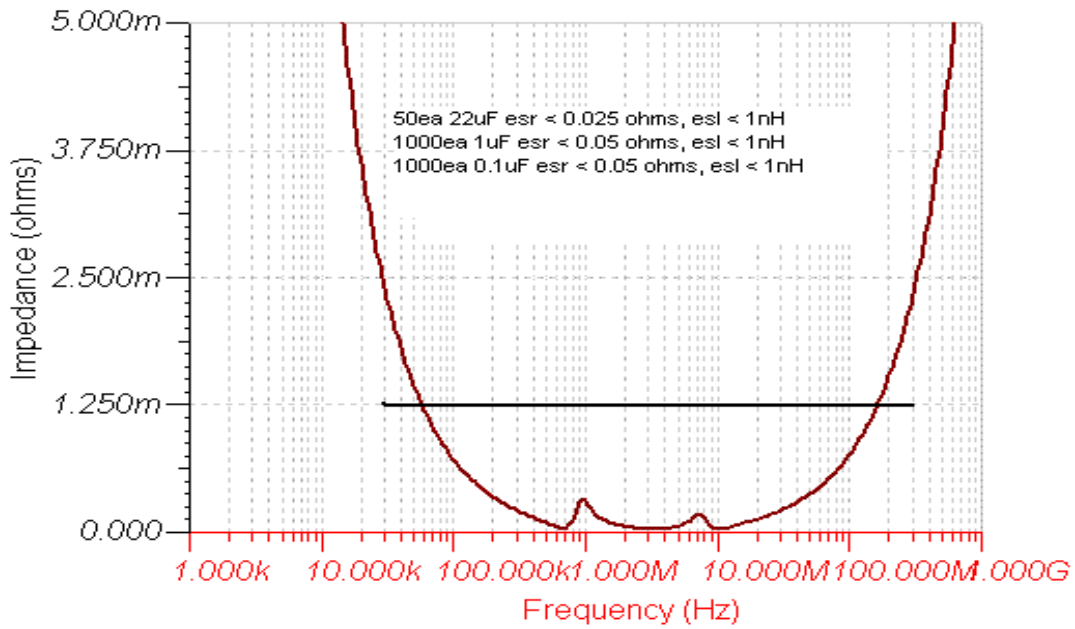


Fig. 4

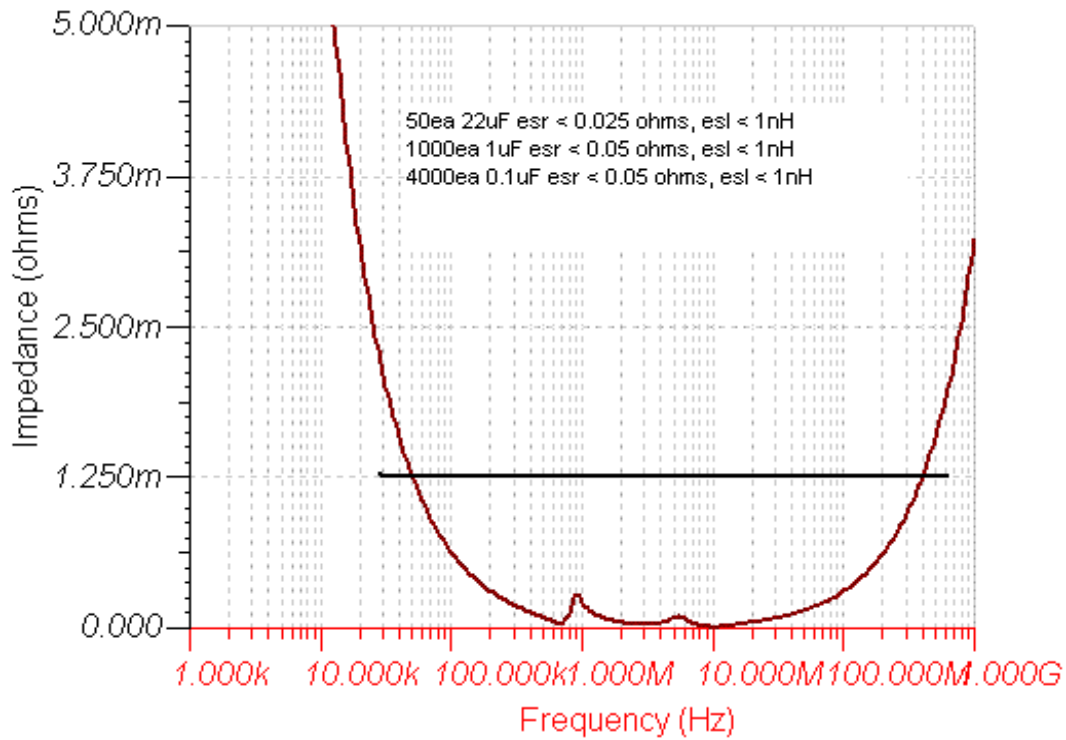


Fig. 5

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The figure 5 decoupling scheme should be used if the 30mV droop/overshoot level is to be achieved for a 1 nsec edge transition on the load change. If higher droop/overshoot is OK for up to 3nsec, the high end of the bandwidth can be relaxed to $f_h = 300/3 = 100\text{MHz}$ and then decoupling shown in figure 3 would be adequate. Alternatively, if the load transition itself is slower than 1nsec, for example, 3nsec. Then the figure 3 decoupling would achieve 30mV of droop/overshoot.

The C_{in} capacitor array is determined in a similar fashion except that the low and high end of the bandwidth is lower in frequency. Use the response time for the particular ATE power supply that is used to determine the lower frequency boundary and use the iPS-SWREG-WS25 response time to figure the upper frequency boundary. Thus $f_l = 300/200000 = 0.0015\text{MHz}$ or 1.5KHz. and $f_h = 300/1000 = 0.3\text{MHz}$. Allow a little overlap on the high end, say 3x or so, giving $f_h = 1\text{MHz}$.

$Z_{in} = 200\text{mV}/25\text{A} = 0.008$ ohms. Total capacitance required is approximately $C_{in} = I (\Delta T/\Delta V) = 25(200\text{usec}/200\text{mV}) = 25,000\text{uF}$. See figure 6 for an example solution. The 1000uF capacitors chosen have an esr of 30 milliohms and esl of 1.5nH.

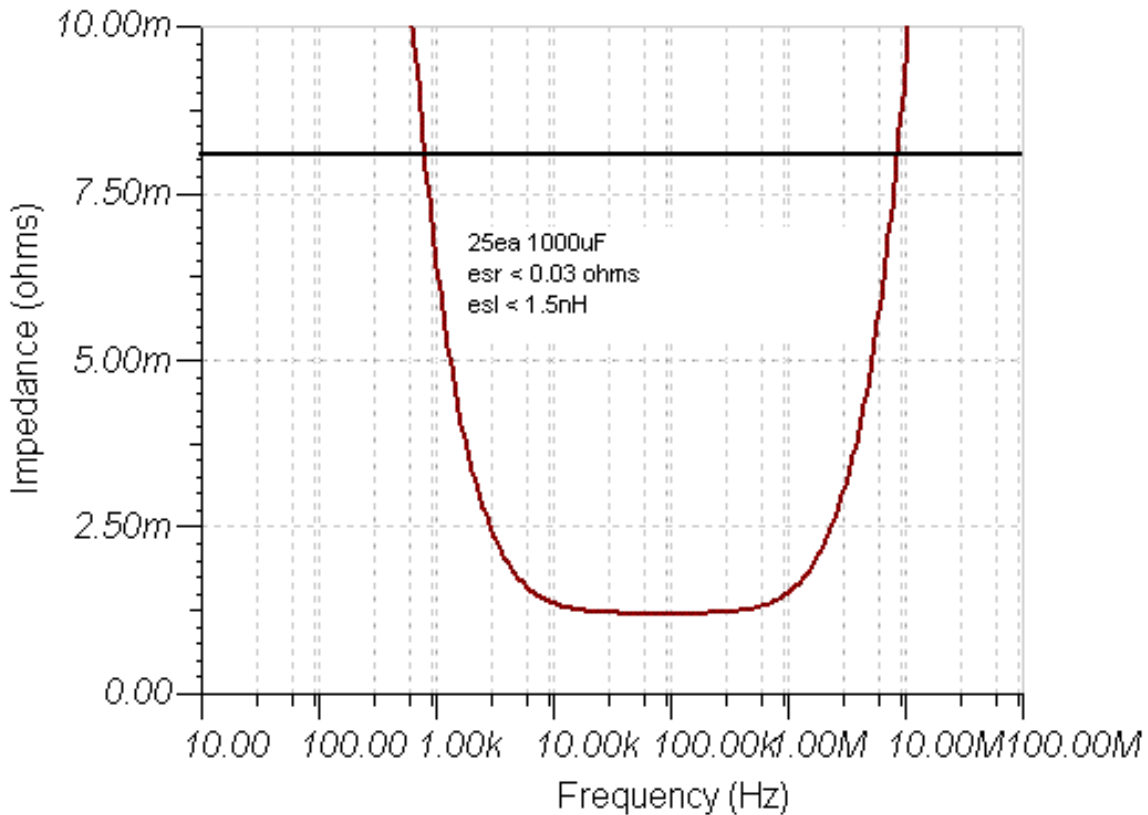


Fig. 6

Regulator 30A/nsec Load Change Simulations

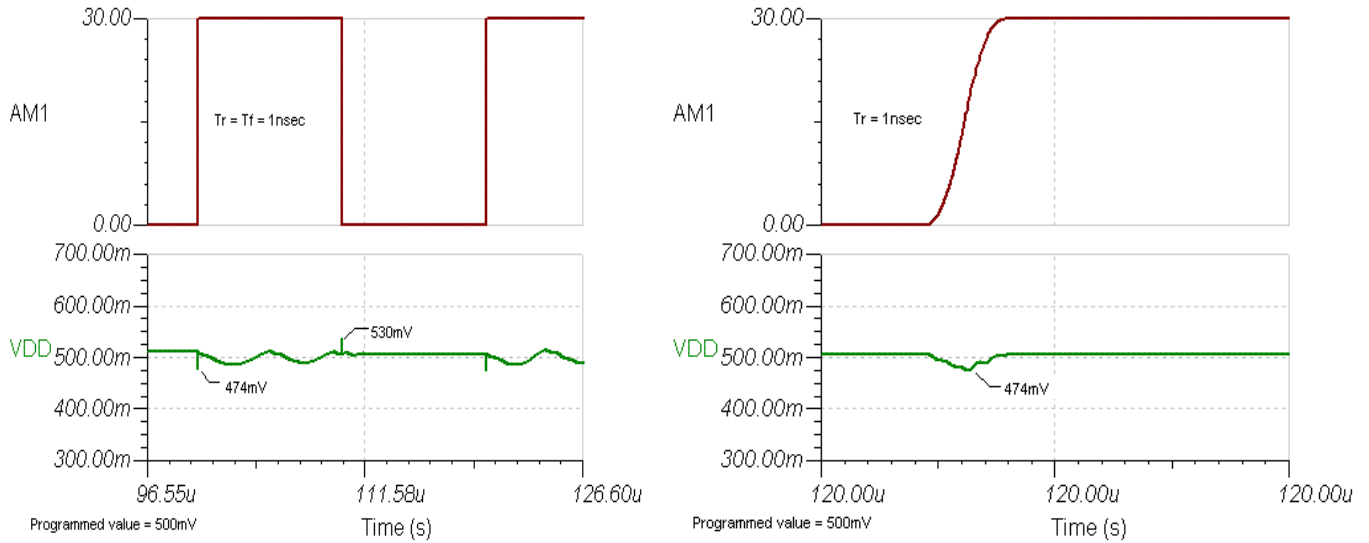


Fig. 7 Load transient 0-30A in Insec using Cin of Fig. 6 and Cout of Fig. 5

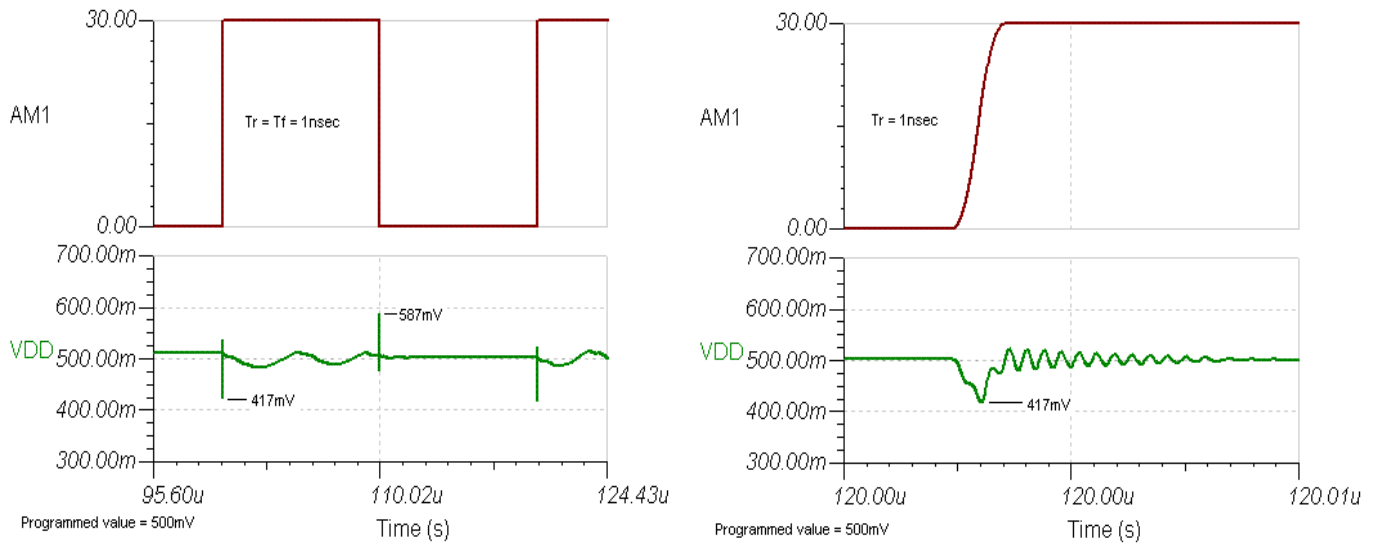


Fig. 8 Load transient 0-30A in Insec using Cin of Fig. 6 and Cout of Fig. 4

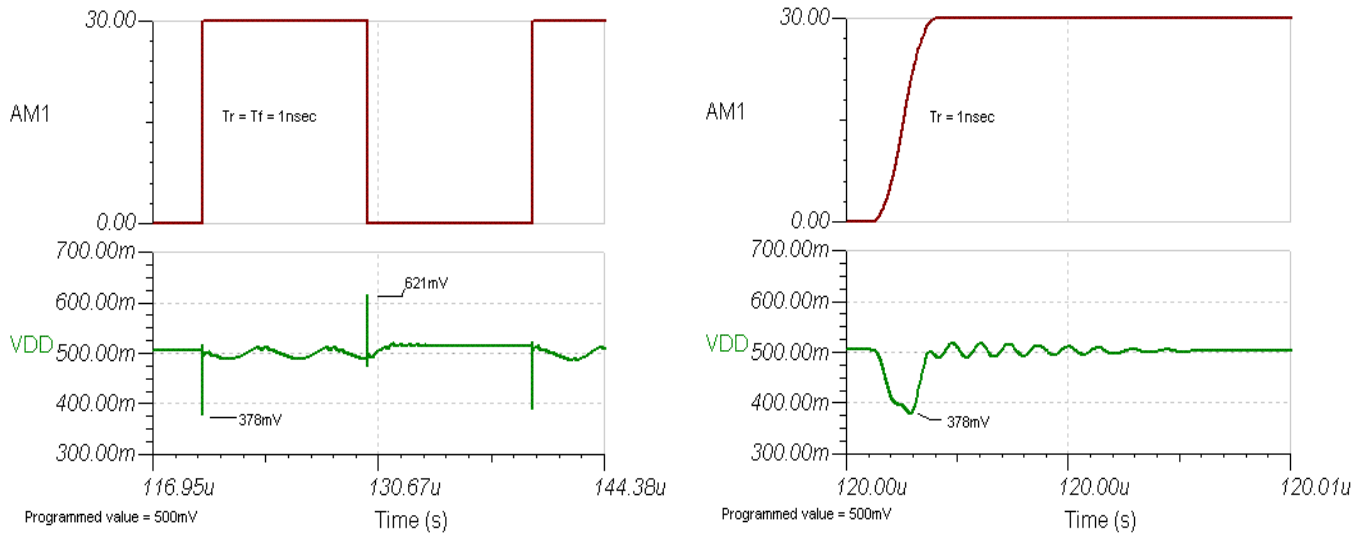


Fig. 9 Load transient 0-30A in 1nsec using Cin of Fig. 6 and Cout of Fig. 3

The voltage droop and overshoot are clearly the best in figure 7 with the Cout capacitor array using the figure 5 capacitor scheme. The droop and overshoot get progressively worse for figures 8 and 9, which correlates with fewer decoupling capacitors as called out in figure 4 and 3 respectively. Notice however that the worst droop and overshoot occur close to the current step edge. If this can be tolerated, then fewer decoupling capacitors are required for the Cout array.



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Regulator Pin Definitions

J1 Pin Definitions

J1-1	Vcc	J1-2	Gnd
J1-3	OTn	J1-4	Gnd
J1-5	Vcc	J1-6	Vcc
J1-7	Vprog	J1-8	Gnd
J1-9	Vsense	J1-10	Gnd
J1-11	Gnd	J1-12	Gnd
J1-13	Gnd	J1-14	Gnd
J1-15	Gnd	J1-16	Gnd
J1-17	Gnd	J1-18	Gnd
J1-19	Gnd	J1-20	Gnd
J1-21	Vdrv	J1-22	Vdrv
J1-23	Vdrv	J1-24	Vdrv

Mating socket for J1: Digikey S6011-12-ND

J2 Pin Definitions

J2-1	Vout	J2-2	Vout
J2-3	Vout	J2-4	Vout
J2-5	Vout	J2-6	Vout
J2-7	Vout	J2-8	Vout
J2-9	Vout	J2-10	Vout
J2-11	Gnd	J2-12	Gnd
J2-13	Gnd	J2-14	Gnd
J2-15	Gnd	J2-16	Gnd
J2-17	Gnd	J2-18	Gnd
J2-19	Gnd	J2-20	Gnd
J2-21	Vin	J2-22	Vin
J2-23	Vin	J2-24	Vin
J2-25	Vin	J2-26	Vin
J2-27	Vin	J2-28	Vin
J2-29	Vin	J2-30	Vin

Mating socket for J2: Digikey S6011-15-ND

